31.5 A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS

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Fully parallel ADC topologies such as a flash ADC are often chosen when the sample rate is high, since they can perform a conversion in a single clock cycle. However, this comes at the expense of an exponential dependence of the area and the power on the resolution, as well as offset variations of the parallel paths. On the other hand, a successive approximation (SA) architecture has only a logarithmic dependence on the resolution and uses only a single comparator, but requires multiple clock cycles to implement the conversion algorithm [1]. By using asynchronous circuitry to achieve single cycle operation and a SA architecture to reduce circuit complexity, a greater than 3 times reduction in the conversion energy per resolution level is achieved over previous high-speed (>10MS/s) ADC implementations. By interleaving this efficient architecture, it is feasible to increase the sample rate to levels usually accomplished by parallel topologies, but with vastly lower power consumption and area.

With two interleaved asynchronous SA ADCs, a peak SNDR of 34dB is achieved at 600MS/s in a 0.13μm CMOS technology. The total power consumption of the ADC is 5.3mW and its die area is 0.12mm^2, including analog, digital, and clock domains. The lower part of Fig. 31.5.1 shows a global 2-phase sampling clock which initiates a sequence of SA comparisons after tracking phase. The clock is synthesized through on-chip regeneration and combination of two external sine waves whose phase skew determines the duty cycle. A data-ready signal is generated upon completion of each comparison and thus avoids the need for the high rate internal clock, which is set to accommodate the worst case comparison resolving time. The asynchronous case removes this constraint as illustrated in Fig. 31.5.1. In fact, since the asynchronous approach eliminates the need for any internal clock, significant power savings are achieved and any extra cycle time penalty due to clock jitter is avoided. This architecture also easily trades off conversion speed with resolution without significant power increase; for example, its power consumption increases from 5.3mW to 5.8mW as sampling rate scales from 600MS/s to 1GS/s while ENOB is reduced by 1.6 bits. Further improvements in conversion rate due to technology scaling will be more easily accomplished by this asynchronous architecture.

To reduce power and increase speed, dynamic open loop circuits are used with a charge redistribution network and a single comparator, as shown in Fig. 31.5.2. This eliminates the need to reduce comparator offset, but slows down the overall conversion speed since the comparator must be reset at each comparison cycle. The input capacitor network is used to sample the input signal and acts as a DAC for creating and subtracting reference voltages. After each comparison, the complementary outputs of the comparator are used by a simple NAND gate to create the ready signal. The transition point of this NAND gate is skewed to eliminate metastability issues arising when the input differential voltage level is small. This ready signal then triggers a block of asynchronous switching logic and temporary bit caches to implement the SA algorithm. A separate pulse generator creates a reset phase for the comparator to avoid any dependence on previous comparisons. Finally, the outputs are written into an on-chip SRAM for self contained testing.

The dynamic comparator is composed of a preamplifier and a regenerative latch, as shown in Fig. 31.5.3. The complementary outputs of the comparator are connected to the positive supply during reset while during evaluation one output is pulled to the negative supply. There are reset switches in both the preamplifier and the latch that help reducing any memory effects as well as allowing input offset cancellation in the preamplifier stage. Current mirrors are used between stages to reduce charge kick back from the logic level swing of the latch onto the small comparator input capacitors.

A non-binary capacitor array (radix 1.81) is used that requires 7 comparison cycles for 6b resolution, which allows extra tolerance for dynamic error through overlapped searching range [2]. While it is desirable to implement this array out of unit elements to preserve matching, this would require a digital ROM which would slow down the conversion process. Alternatively, a geometric-scaled capacitor array can be used for higher conversion rate but the matching requirement will be more stringent. By using a non-binary capacitive ladder network as shown in Fig. 31.5.4, it is possible to create a non-binary radix with only 3 different sizes with ratios $1{:}\alpha{:}\beta$. The series connection also has the advantage of dramatically reducing the effective input capacitance in this design to 90fF. The effect of the parasitic capacitance associated with the floating nodes can be reduced since the ratio α can be increased while maintaining the intended non-binary ratio. A foreground off-chip calibration scheme is used to determine the appropriate combination weights to compensate for the unpredicted parasitic capacitances and capacitor mismatch. With the ability to compensate for parasitic capacitances, metal-oxide-metal (MOM) capacitors are thus used rather than MIM capacitors.

The measured results (Fig. 31.5.5) show ENOB of a single ADC scales from 5.3b at 300MS/s to 3.7b at 500MS/s. The design of the clock network and DAC allows the use of sub-sampling, so that with a sampling frequency of 300MHz, the SNDR remains above 30dB even with an input frequency of over 4GHz. This ability to directly sample RF signals makes a sub-sampling front end practical [3].

Since a single ADC occupies an area of 250×240μm^2, it is attractive to use parallel ADCs with time interleaving to increase the sampling rate. Figure 31.5.6 shows the data for two ADCs interleaved on-chip to achieve a 600MS/s rate at twice the power. Off-chip subtraction of each ADC offset removes spurious tone for SNDR improvement of 0.7dB. There is little reduction of SNDR at lower frequency, but as the input frequency increases above 300MHz, the clock skew between paths yields a several dB SNDR reduction which can be alleviated by additional calibration. With FOM defined as total power/($2^{ENOB}\times f_s$), these interleaved ADCs achieve 0.22pJ/conversion-step at 600MS/s, with analog, digital, and clock section consuming 1.2mW, 3.2mW, and 0.9mW, respectively. The total die size including pads is 1.4×1.74mm^2 (Fig. 31.5.7).

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[1] D. Draxelmayr, "A 6b 600 MHz 10mW ADC Array in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 264-265, Feb., 2004.
[2] F. Kuttner, "A 1.2V 10b 20Msample/s Non-Binary Successive Approximation ADC in 0.13 um CMOS," *ISSCC Dig. Tech. Papers*, pp. 176-177, Feb., 2002.
[3] M. S.W. Chen and R. W. Brodersen, "A Subsampling UWB Radio Architecture by Analytic Signaling," *Proc. ICASSP*, vol. 4, pp.533-536, May 2004.

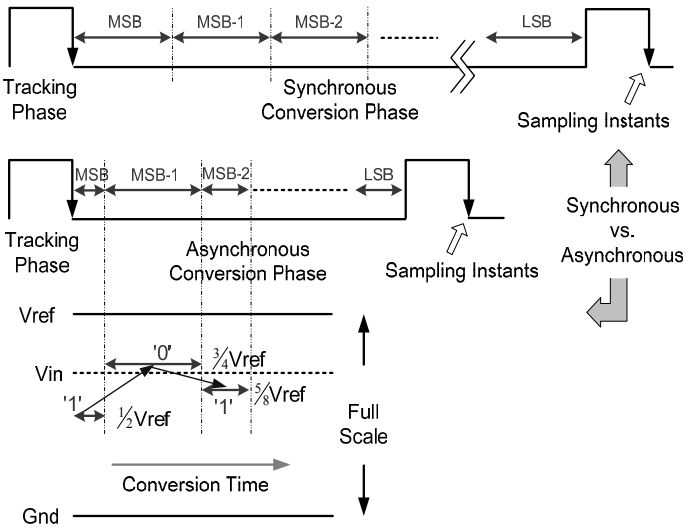


Figure 31.5.1: Reduction of conversion time by asynchronous comparisons.

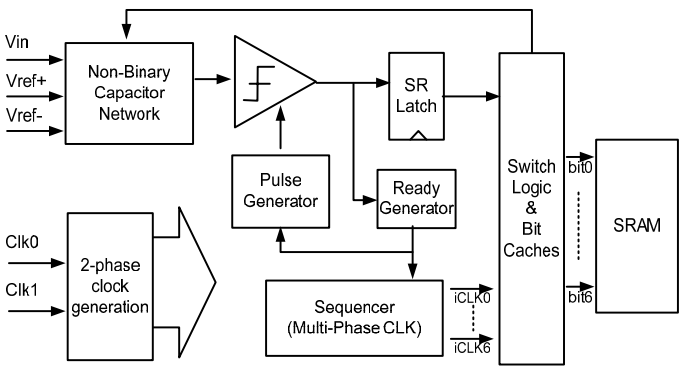


Figure 31.5.2: Single asynchronous ADC architecture.

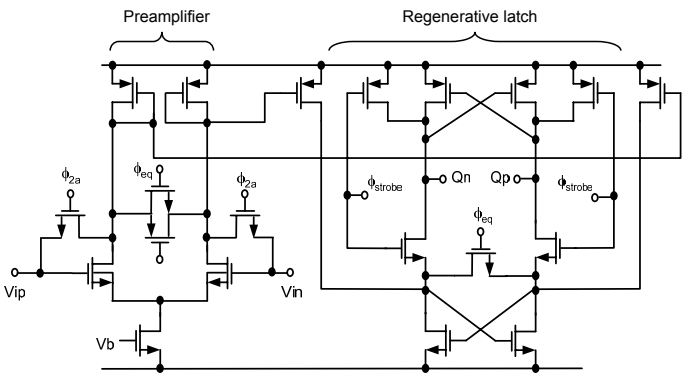
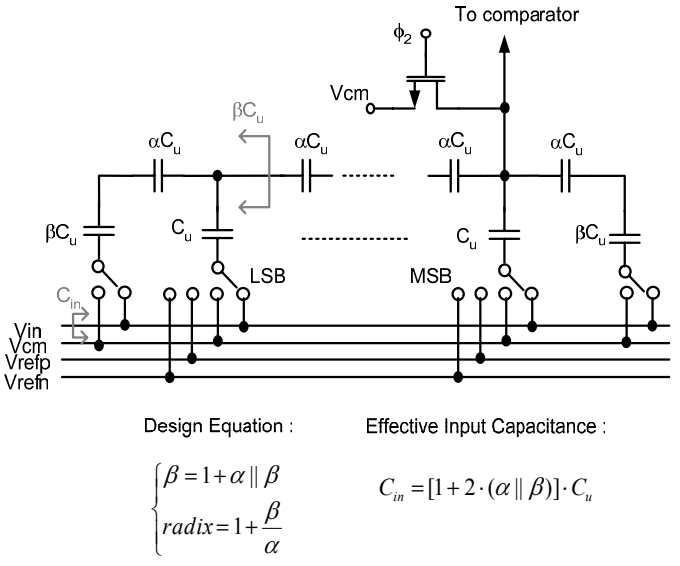


Figure 31.5.3: Schematic of comparator.



$$\begin{cases}\beta = 1+\alpha \,\|\, \beta \\ radix = 1+\dfrac{\beta}{\alpha}\end{cases}$$

$$C_{in} = [1+2\cdot(\alpha \,\|\, \beta)]\cdot C_u$$

Figure 31.5.4: Non-binary capacitive ladder network.

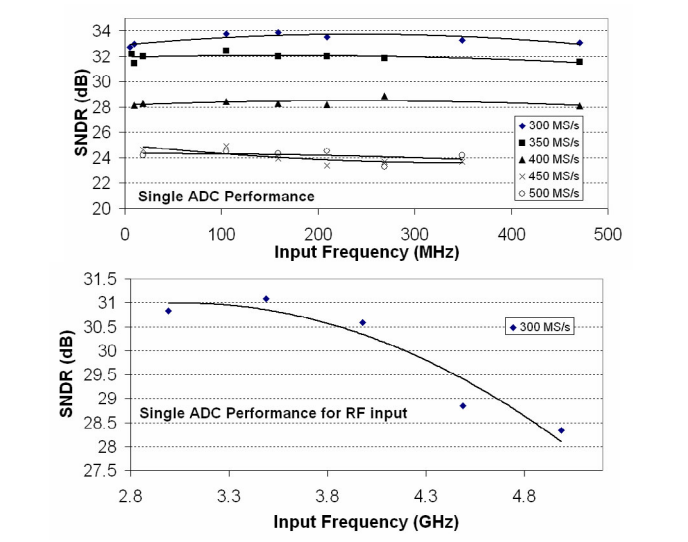


Figure 31.5.5: Measured SNDR versus f_s and f_{in} (up to 5GHz) for single ADC.

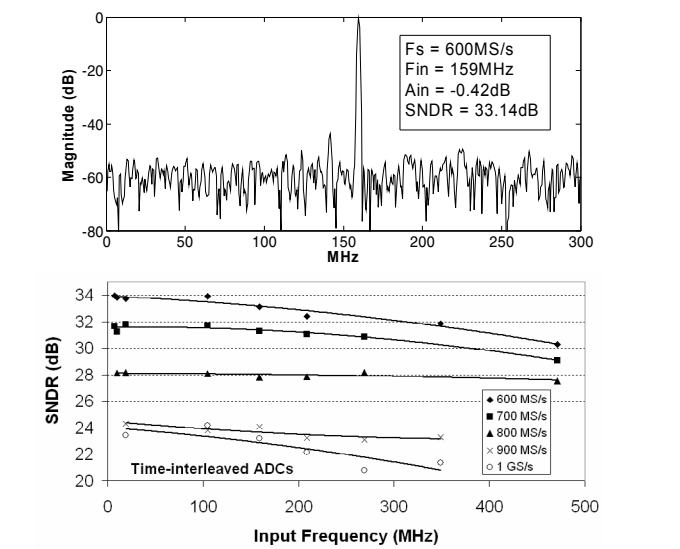


Figure 31.5.6: Measured FFT spectrum and SNDR versus f_s and f_{in} for dual ADCs.

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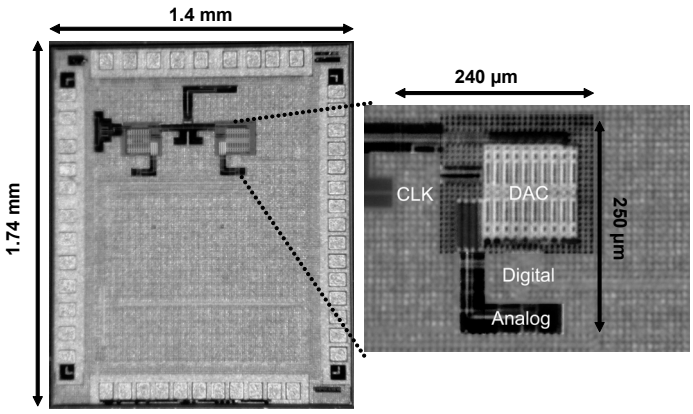

Figure 31.5.7: Die micrograph.

